Entner Electronics
ERIC5
9bit Soft-Core CPU for FPGAs

About Soft-Core CPUs

Unlike traditional CPUs or micro-controllers, soft-core CPUs are implemented into FPGAs. You get either a netlist or a HDL-design from the soft-core vendor and can use this for integration into your own FPGA design.

Because many electronic designs are already using FPGAs and also a traditional microcontroller, there is the possibility to remove the external microcontroller and thus reduce the PCB area and production costs.

Another advantage is the great design-flexibility. You can add exactly the peripherals you require to your design. Therefore you do not have to pay for unnecessary peripherals and you can create your own custom mix of functions. If you e.g. require 28 PWM channels and 4 UARTs, you may not find an off-the-shelf microcontroller that provides this while with a soft-core-CPU this is not a problem.
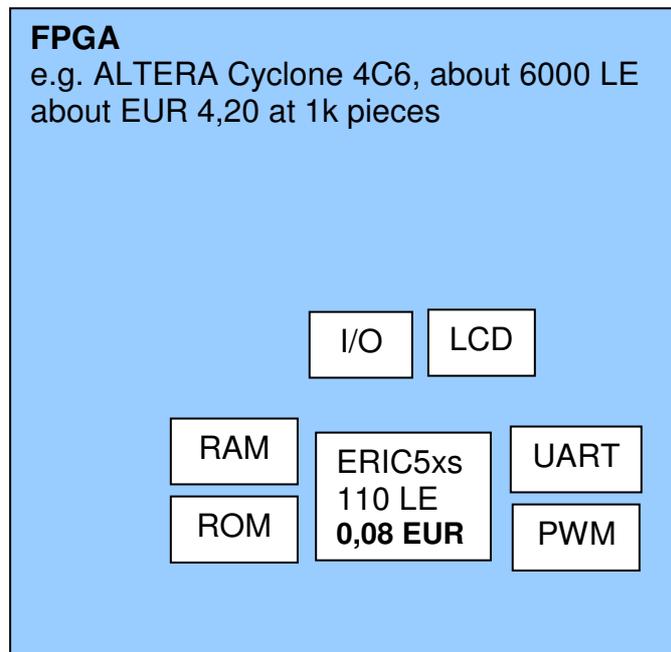
Additionally, FPGA-vendors are very aggressively adopting newest process-technologies where the soft-cores fully benefit from. This overcompensates the overheads of the "soft" implementation when compared to low-cost microcontrollers.

And last but not least, there is no risk of product-discontinuance, especially if you have the HDL-code of the soft-core CPU.

Features of ERIC 5

- Extremely small size: The size of ERIC5xs is e.g. about 110 logic elements in the ALTERA Cyclone-family, which is less than 5% of the smallest family-member. This results in calculated costs well below 40 cents - practically ERIC5 is "for free" in most FPGA-designs.
- Optional multiplier-support to make use of the hardware multipliers available in most modern FPGAs.
- Vendor independent: Unlike most other soft-cores, especially the ones from the FPGA vendors themselves, ERIC5 is not optimized for a specific FGPA architecture. This makes ERIC5 usable in all major FPGAs (and also ASICs), which in turn makes your design reusable even when you decide to change your FPGA vendor!
- Low cost: No "per-unit" license-fees, you get full VHDL-code for maximum independence.
- Development tools: C-compiler with optimizer and command-line assembler are available.

Design for Low Cost

FPGA
e.g. ALTERA Cyclone 4C6, about 6000 LE
about EUR 4,20 at 1k pieces

| I/O | LCD |

| RAM | ERIC5xs 110 LE **0,08 EUR** | UART |
| ROM | | PWM |

ERIC5 is targeted for low-cost designs with a small FPGA.

As you can see in this example, a typical ERIC5xs will "cost" 8 cents, while a full-featured ERIC5Q+ would still be well below 40 cents. Please note that this is based on "real life" pricing, not on e.g. 250k-pricing in one year's time.

The area of the peripherals also needs to be considered. The solutions from Entner Electronics are all optimized for area and are typically very small.

Family members

There are four family-members that differ by following features:

	ERIC5xs	ERIC5Q	ERIC5+	ERIC5Q+
Opcode Width	8bit	8bit	9bit	9bit
9bit Registers	3	4*	3	4*
Max. Code-Size	1k recommended (128kB possible)	128kB	1k recommended (512kB possible)	512kB
Max. Data-Size	0.5 kB	0.5 kB	0.5 kB	0.5 kB
Typ. Fmax	60 MHz	60 MHz	60 MHz	60 MHz
Typ. MIPS	25	25	40	40
Multiplier	opt. (18 x 9/18)	opt. (18 x 9/18)	opt. (18 x 9/18)	opt. (18 x 9/18)
Interrupts	n/a	supported	n/a	supported
C-support	no	yes	no	yes

* the 4th register is the Q-register which is typically used as a stack-pointer

Preliminary information – specification and availability subject to change without notice